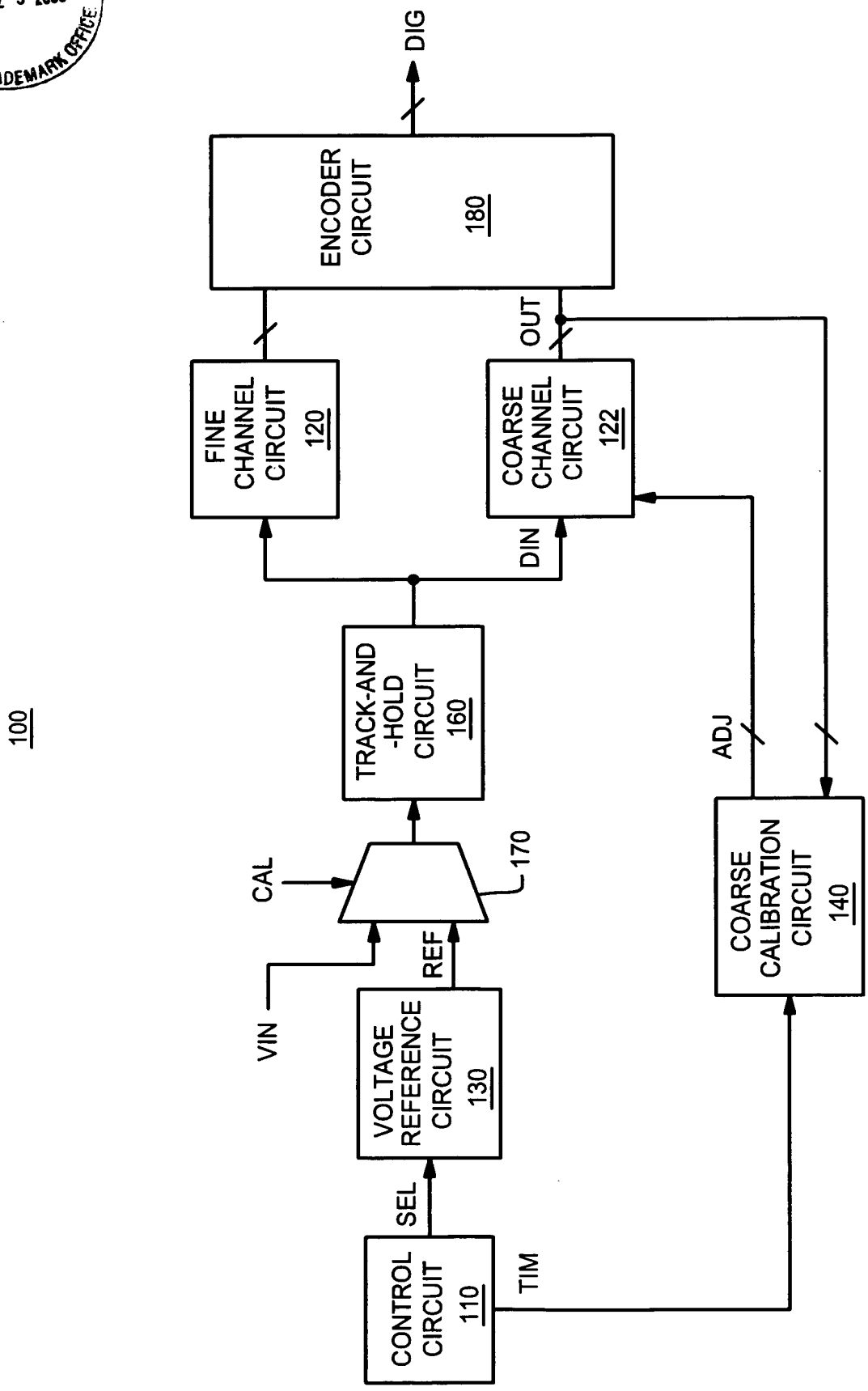


Figure 1

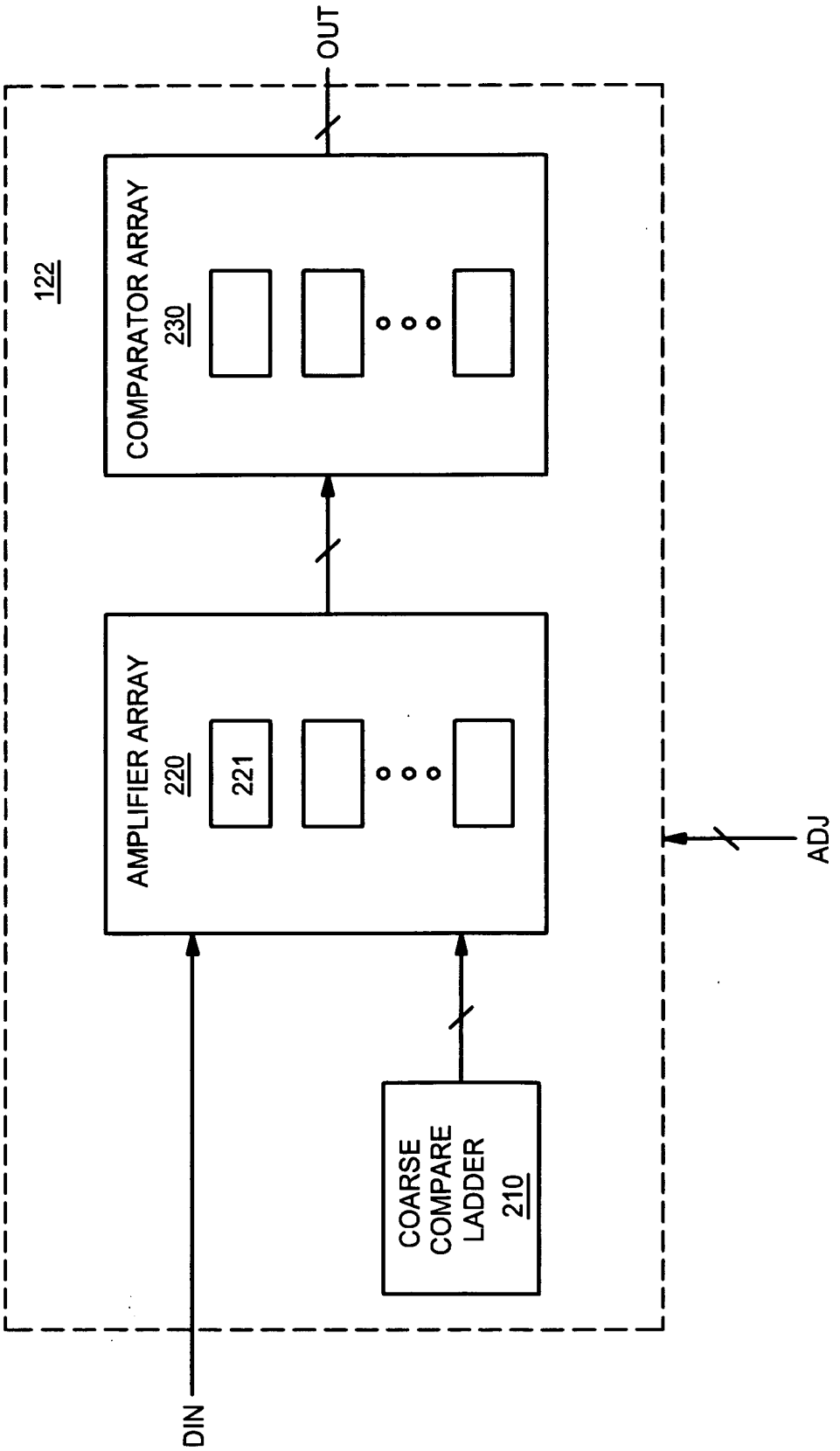

OUT
122
COMPARATOR ARRAY
230
AMPLIFIER ARRAY
220
221
ADJ
COARSE
COMPARE
LADDER
210
DIN

Figure 2

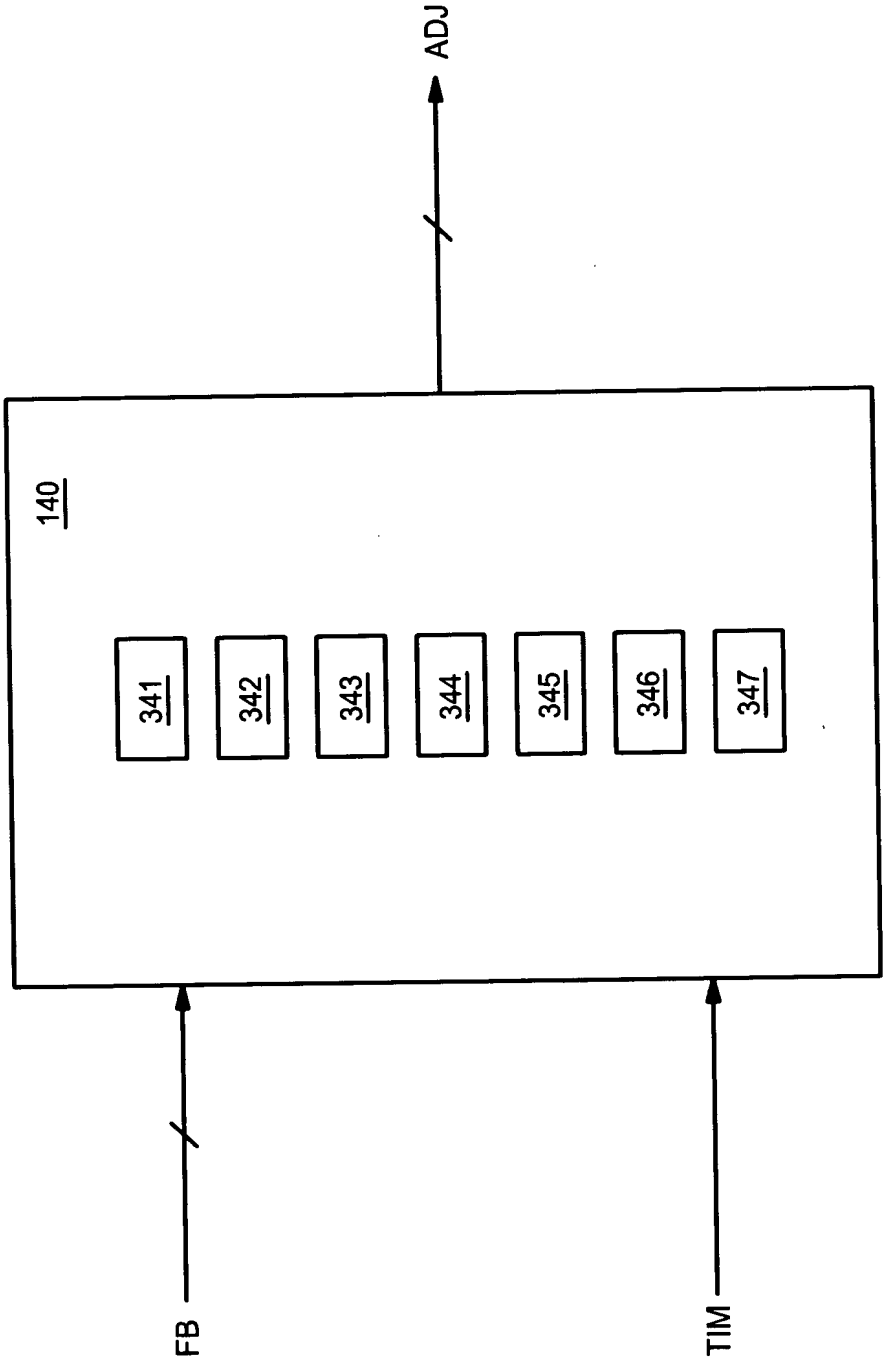


Figure 3A

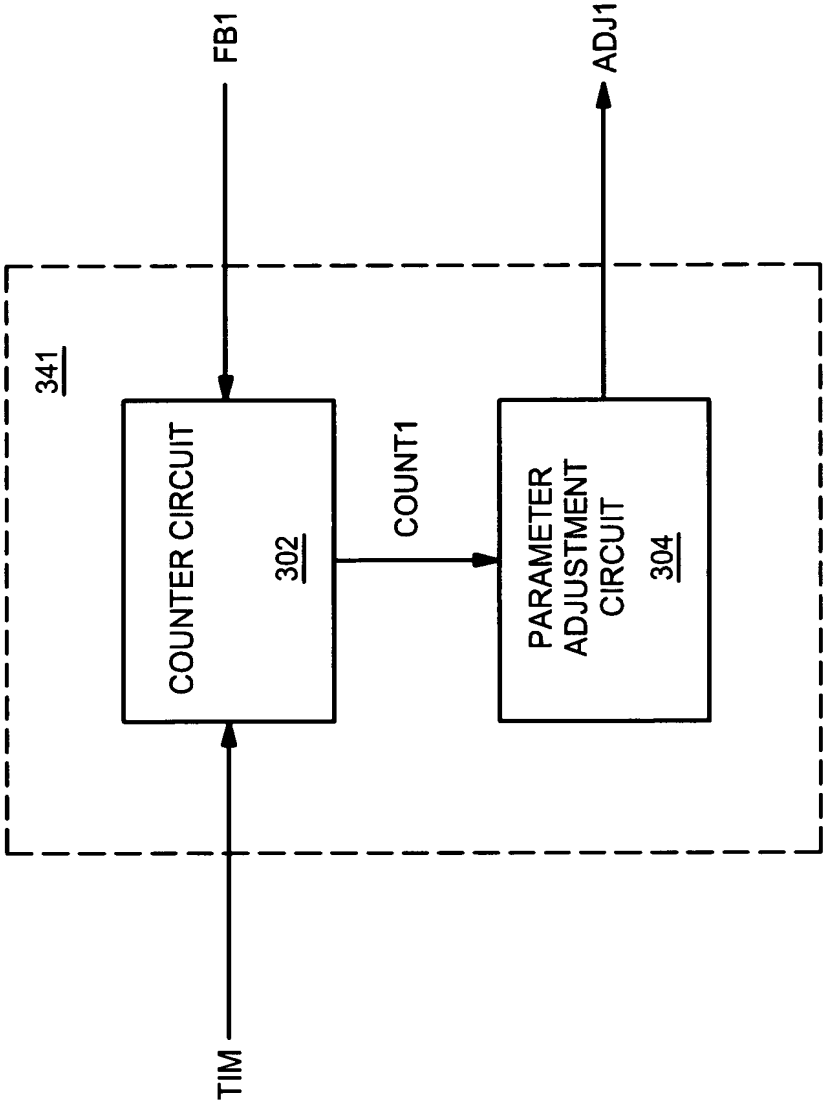

FB1
ADJ1
341
COUNTER CIRCUIT
302
COUNT1
PARAMETER
ADJUSTMENT
CIRCUIT
304
TIM

Figure 3B

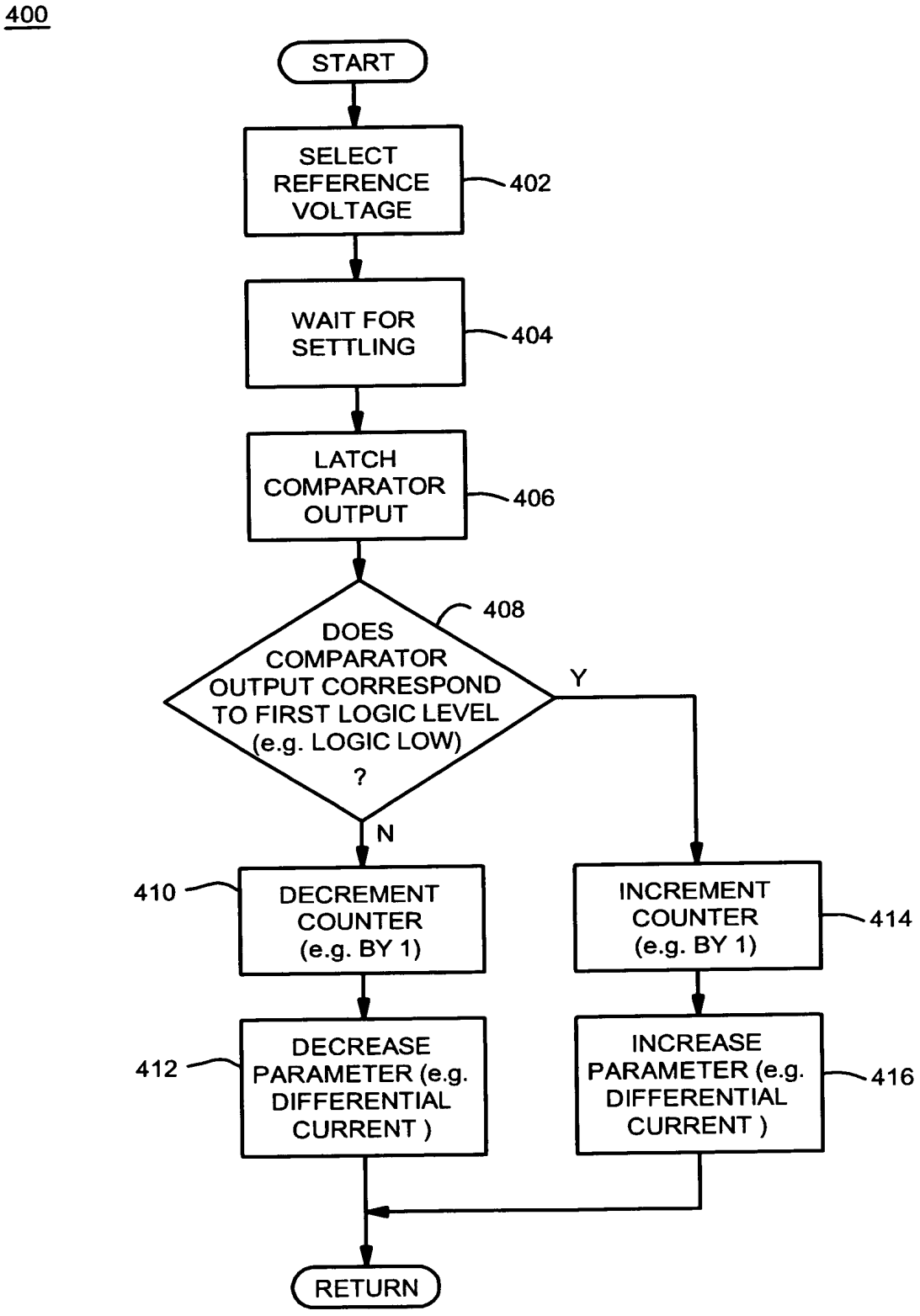

400
START
SELECT REFERENCE VOLTAGE
402
WAIT FOR SETTLING
404
LATCH COMPARATOR OUTPUT
406
408
DOES COMPARATOR OUTPUT CORRESPOND TO FIRST LOGIC LEVEL (e.g. LOGIC LOW) ?
Y
N
410
DECREMENT COUNTER (e.g. BY 1)
412
DECREASE PARAMETER (e.g. DIFFERENTIAL CURRENT)
INCREMENT COUNTER (e.g. BY 1)
414
INCREASE PARAMETER (e.g. DIFFERENTIAL CURRENT)
416
RETURN

Figure 4

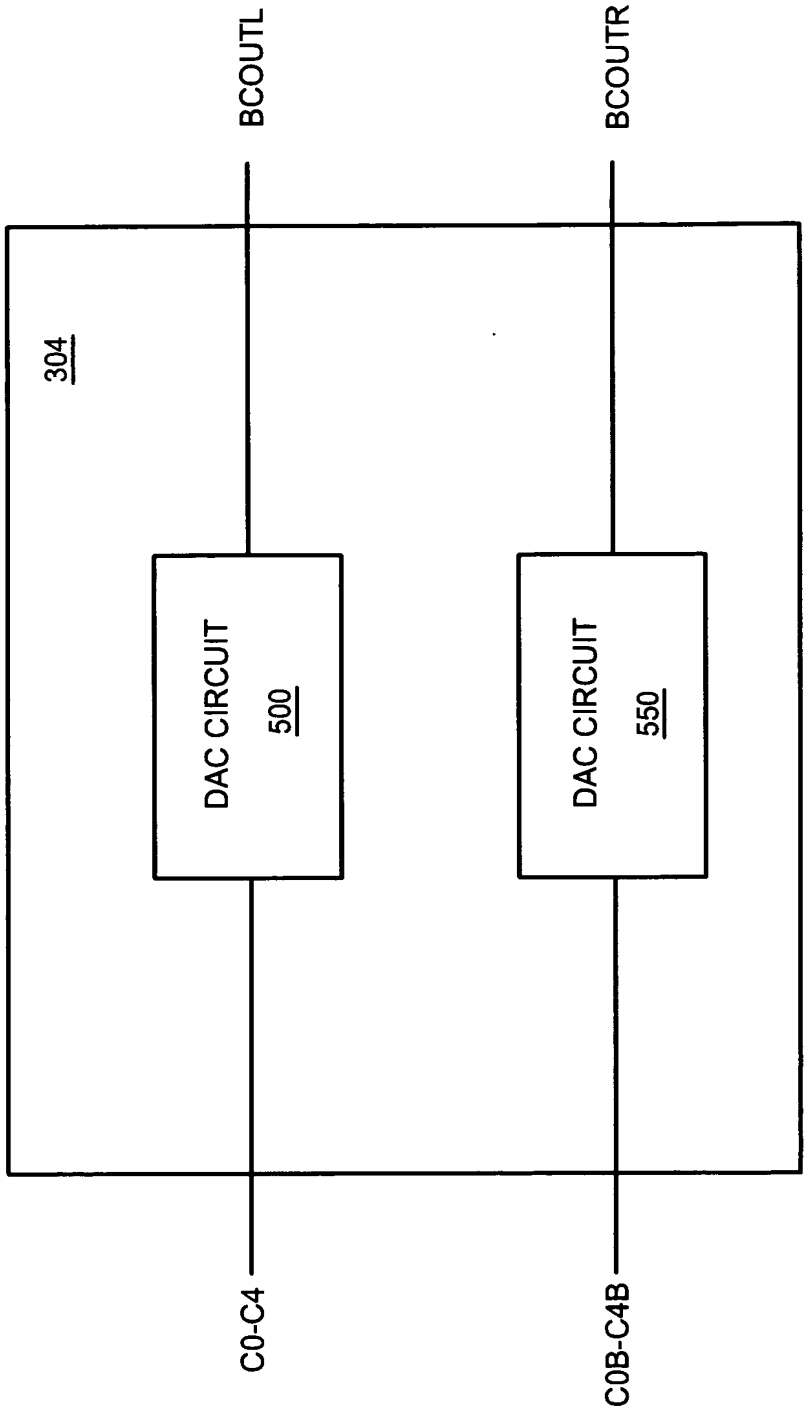

BCOUTL
BCOUTR
304
DAC CIRCUIT
500
DAC CIRCUIT
550
C0-C4
C0B-C4B

Figure 5A

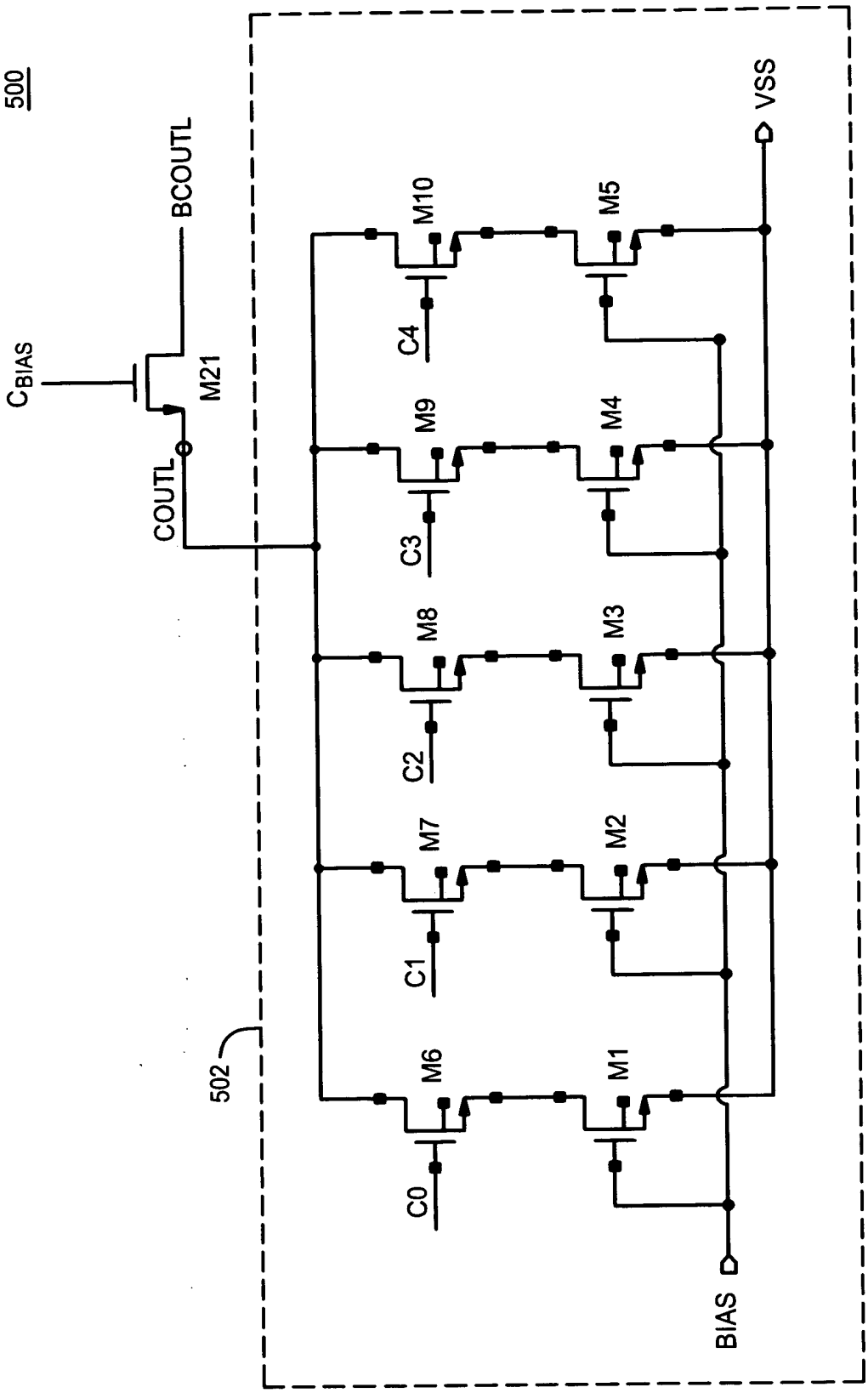
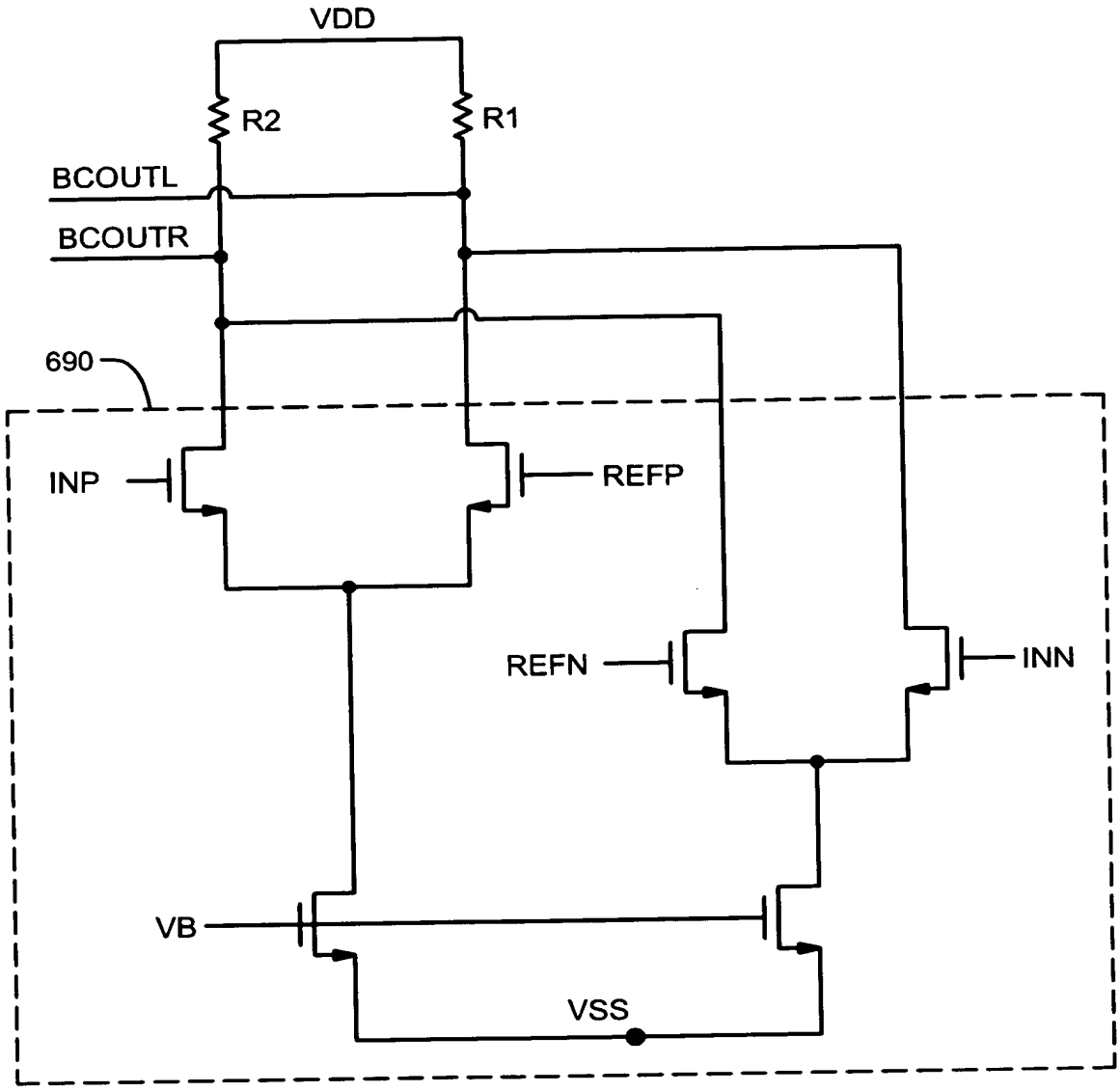

500
BCOUTL
VSS
M10
M5
C4
C_{BIAS}
M21
M9
M4
COUTL
C3
M8
M3
C2
M7
M2
C1
502
M6
M1
C0
BIAS

Figure 5B

221



INP ( ) AND INN ( ) = DIN

Figure 6